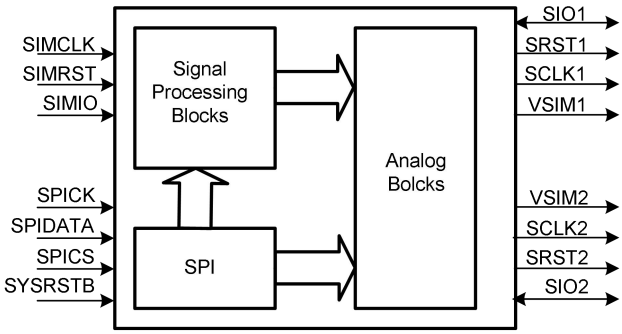
GT4302
Dual SIM Card Controller

1 Features	2 Application
- Control and communication through a SPI interface with baseband processor. **- CMOS technology for dual SIM card controlling** **- Power management and control for two SIM cards** **- Independent 1.8/3V V_{CC} control for each SIM card** **- Fast channel switching** **- Independent clock stop mode (at high or low level) for each SIM card** **- Temperature Range: –40°C to 85°C** **- 20-pin 3mm x 3mm QFN package (Pb-free & Green available):**	**- GSM** **- EDGE** **- GPRS** **- LTE Cell Phones**

3 Description	Circuit Diagram
The GT4302 is a dual SIM card control chip optimized for GSM/EDGE/GPRS/LTE handsets, It provides the power conversion and signal level translation needed for advanced cell phones to interface with 1.8V and 3V SIMs. The device meets all requirements for 1.8V and 3V SIMs and contains LDO regulators to power 1.8V or 3V SIM card from a 2.7V to 5.5V input. A serial port interface(SPI) is used to control dual SIM channel individually. The GT4302 I/O voltage can support 1.65V to 5.5V. The GT4302 is available in 20-pin 3mm x 3mm QFN package. The operating temperature range is from -40°C to +85°C.	

4 Revision History

Revision	Date	Note
Rev. A0. 1	2024. 12. 20	Original Version
Rev. A1. 0	2025. 04. 30	Official Version
Rev. A1. 1	2025. 06. 09	Updated Electrical Specifications

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table.5-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)	MSL(3)	Package Qty
GT4302	GT4302QSG	QFN3*3-20L	3.00mmx3.00mmx0.75mm	GT4302 XXXXX	3	Tape and Reel,5000

(1)For all available packages, please contact product sales.

(2)There may be additional marking, which relates to the lot trace code information (data code and Vendor code), the logo or the environmental category on the device.

(3)MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4)"XXXXX" in Marking will be appeared as the batch code.

5 Device Summary, Pin and Packages(Continued)

Top View

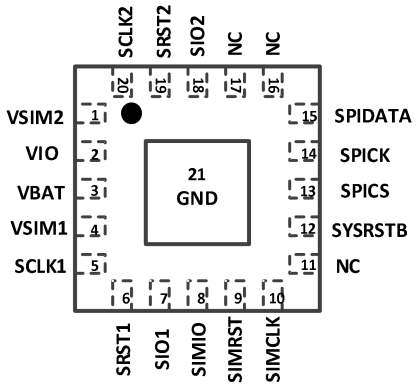


Fig.5-1. GT4302: QSG (QFN3×3-20L) Package

Table.5-2. Pin Definition

PIN		I/O	Description
Name	S6 C6		
VSIM2	1	O	SIM2 Supply
VIO	2	-	Digital IO Supply
VBAT	3	-	Battery Input Voltage
VSIM1	4	O	SIM1 Supply
SCLK1	5	O	Level-Shifted SIM1 Clock Output
SRST1	6	O	Level-Shifted SIM1 Reset Output
SIO1	7	I/O	Level-Shifted SIM1 Bidirectional Data Input/Output
SIMIO	8	I/O	Non-Level-Shifted Bidirectional Data I/O
SIMRST	9	I	Non-Level-Shifted SIM Reset Input
SIMCLK	10	I	Non-Level-Shifted SIM Clock Input
NC	11		
SYSRSTB	12	I	System Reset, Low Active
SPICS	13	I	Serial bus selection
SPICK	14	I	Serial bus clock
SPIDATA	15	I	Serial bus data
NC	16		
NC	17		
SIO2	18	I/O	Level-Shifted SIM2 Bidirectional Data Input/Output
SRST2	19	O	Level-Shifted SIM2 Reset Output
SCLK2	20	O	Level-Shifted SIM2 Clock Output
GND	21	-	Ground

* All unused input pins cannot be suspended and suggested to connect to GND.

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings(1)

Parameters	Min	Max	Unit
Supply voltage, V_{VIO}	-0.3	6	V
Supply voltage, V_{BAT}	-0.3	6	V
DC Switch Voltage,V_S	-0.3	6	V
DC Input Voltage,V_{IN}	-0.3	6	
Maximum junction temperature		150	°C
Storage temperature range	-65	150	°C
Maximum power consumption(P_D) @+85°C		180	mW

(1)Absolute Maximum Ratings may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

6.2 ESD Ratings(1) (2)

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-Body Model (HBM)	3K	V
		Charged-Device Model (CDM)	2K	V

(1)JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Electrical Specifications

Typical values are at TA=+25ºC, VIO=3.0V, VBAT=4.0V, C_{VREF}=C_{VSIM1}=C_{VSIM2}=2.2uF, minimum loads applied on all outputs.(unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Unit
Input power supply					
VBAT Operating Voltage		2.7		5.5	V
VBAT Shutdown Current	VIO=0V		0.1	1	uA
VBAT Operating Ground Current	VSIM1=3.0V, VSIM2=0V, no load		25	50	uA
	VSIM1=1.8V, VSIM2=0V, no load		25	50	
VIO Operating Voltage		1.65		5.5	V
VIO Shutdown Current			0.1	1	uA
VIO Operating Ground Current			3	5	uA
Input Control					
Low Input Threshold	SPIDATA, SPICK, SPICS, SYSRSTB			0.15*VIO	V
High Input Threshold	SPIDATA, SPICK, SPICS, SYSRSTB	0.85*VIO			V
SIM Card Supplies (VSIM1, VSIM2)					
1.8V Output Voltage		1.65	1.8	1.95	V
3.0V Output Voltage		2.82	3.0	3.18	V
Output Short Current Limit			38		mA
Load Regulation(1.8V)	0.05mA<I_load<20mA at VBAT=3.6V		4	6	mV
Load Regulation(3.0V)			5	7	
Turn-On Time	No load, Enable to VSIM1,2 at 90% selected voltage		0.8	1.5	ms
GSM Interface					
Vih(SIMCLK, SIMRST)		Vio-0.6			V
Vil (SIMCLK, SIMRST)				0.6	V
Vil (SIMIO)	Vol<=0.4V, Iol=1mA			0.223	V
	Vol<=0.4V, Iol=0mA			0.335	
Vih(SIMIO), Voh(SIMIO)	Iih, Ioh=±20uA	Vio-0.6			V
Iil(SIMIO)	Vil=0V			0.9	mA
Vo(SIMIO)	Vil=0.4V			0.47	V
Interface to 3V SIM Card					
Vol(SRST)	Sink Current=-20uA (VSIMRST=0.6V)			0.4	V
Voh(SRST)	Source Current=200uA(VSIMRST=Vio-0.6V)	0.9*VSIM			V
Vol(SCLK)	Sink Current= -20uA (VSIMCLK=0.6V			0.4	V
Voh(SCLK)	Source Current=200uA(VSIMCLK=Vio-0.6V)	0.9*VSIM			V
Vil(SIO)				0.15*VSIM	V
Vih(SIO), Voh(SIO)	Source Current=20uA	VSIM-0.4			V
Iil(SIO)	VSIO=0V			-1	mA
Vol(SIO)	Sink Current=-1mA(VSIMIO=0V)			0.15*VSIM	V
Interface to 1.8V SIM Card					
Vol(SRST)	Sink Current=-20uA(VSIMRST=0.6V)			0.2*VSIM	V
Voh(SRST)	Source Current=200uA(VSIMRST=Vio-0.6V)	0.9*VSIM			V

7 Electrical Specifications(Continued)

Parameter	Condition	Min	Typ	Max	Unit
Vol(SCLK)	Sink Current= -20uA (VSIMCLK=0.6V			0.2*VSIM	V
Voh(SCLK)	Source Current=200uA(VSIMCLK=Vio-0.6V)	0.9*VSIM			V
Vil(SIO)				0.15*VSIM	V
Vih(SIO), Voh(SIO)	Source Current=20uA	VSIM-0.4			V
Iil(SIO)	VSIO=0V			-1	mA
Vol(SIO)	Sink Current=-1mA(VSIMIO=0V)			0.15*VSIM	V
SIM Card Interface Timing					
SRST, SIO rise/fall times	VSIM=3,1.8V, loaded with 30pF (10%~90%)		60	350	ns
SCLK rise/fall times	VSIM=3V, loaded with 30pF(10%~90%)		7	15	ns
	VSIM=1.8V, loaded with 30pF (10%~90%)		15	25	ns
SCLK frequency		5			MHz
SCLK duty cycle	SIMCLK Duty=50%, fSIMCLK=5MHz	47		53	%
SCLK propagation delay	From SIMCLK to SCLK, load with30pF		14	30	ns

8 Detailed Description

The GT4302 is a dual-channel SIM card power management and level shifter with serial (SPI) interface. It mainly consists of the following basic modules:

- Serial Port Interface Module
- Control Module
- LDO Regulators
- Level shifters

8.1 Serial Port Interface (SPI)

This module is used to receive the commands transmitted by baseband processor. It will decode the received data and send corresponding commands to signal processing and analog blocks. The 8-bit serial interface uses three pins –SPICS#, SPIDATA and SPICK to enter data. Data read is not available with the serial interface and data entered must be 8 bits. The description of three pins is:

Signal Name	Attribute	Direction	Description
SPICK	Edge Triggered	BB->GT4302	Serial bus clock
SPIDATA	Level	BB->GT4302	Serial data
SPICS	Active Low	BB->GT4302	SPI bus selection

Fig. 8-1 shows the timing diagram of this serial interface. When the block is idle, SPICK is forced LOW and SPICS# is forced HIGH. Once the data register contains data and the interface is enabled, SPICS# is pulled LOW and remains LOW for the duration of the transmission. The first three bits are address bits and the others are data bits.

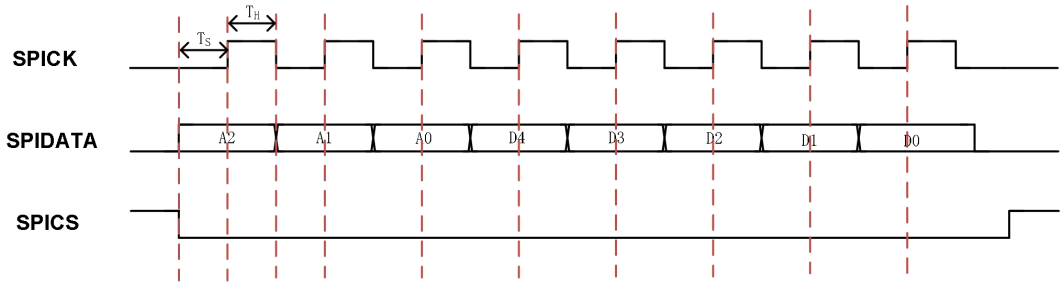


Fig.8-1. SPI Interface Transfer Diagram

Serial Port Interface Timing:

Symbol	Parameter	Min	Tye	Max	Unit
Ts	SPIDATA to SPICK setup time	4			ns
Th	SPIDATA to SPICK hold time	4			ns

8.2 Register Definitions:

A[2:0]: register address definition:

A2	A1	A0	Register name
0	0	0	Reset Control Register
0	0	1	SPICLK Control Register
0	1	0	SPIDATA Control Register
0	1	1	VSIM Control Register

8 Detailed Description(Continued)

D[4:0]: register data definition:

0000H Reset control Register

Bit	4	3	2	1	0
Name		RSTVAL		RSTSEL	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd.

RSTSEL SIM card RST pin control, only valid when VCCEN is 1.

0 The RST pin of SIM card is the same as GT4302 input pin SIMRST.

1 The RST pin of SIM card is controlled by RSTVAL as show below.

RSTVAL Control the value of SIM card RST pin, only valid when VCCEN is 1 an RSTSEL is 1.

0 Force the SIM card RST pin to 0.

1 Force the SIM card RST pin to 1.

0001H Clock Control Register

Bit	4	3	2	1	0
Name		CPOH		CPOL	
Type		WO	WO	WO	WO
Reset		0	0	1	1

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one.

CPOH,CPOL The value of SIM card pin is controlled by the combination of the two signals when VCCEN is 1.

01 The CLK pin of SIM card is the same as GT4302 input pin SIMCLK.

11 Force the SIM card CLK pin to stop at high.

00 Force the SIM card CLK pin to stop at low.

10 Not allowed.

0002H Data Control Register

Bit	4	3	2	1	0
Name		DATA_L		DATAEN	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one.

DATAEN SIM card DATA pin control, only valid when VCCEN is 1.

0 The channel between SIM card DATA pin and GT4302 I/O pin SIMDATA will be gapped. If there were no drivers of these two pins, the they will be pulled high.

1 The channel between SIM card DATA pin and GT4302 I/O pin SIMDATA will be opened. If there

8 Detailed Description(Continued)

Were no drivers of these two pins, then they will be pulled high.

DATA_L Control the value of SIM card DATA pin, only valid when both VCCEN and DATAEN are 1.

0 Normal function.

1 Force the SIM card DATA pin to 0.

0003H V_{CC} Control Register

Bit	4	3	2	1	0
Name		VCCEN		VSEL	
Type		WO	WO	WO	WO
Reset		0	0	0	0

The LSB of these two signals is for 1st SIM card, and MSB is for 2nd one.

VCCEN SIM card power control.

0 Turn off SIM card V_{CC} pin, all signals to SIM card will be 0.

1 Turn on SIM card V_{CC} pin.

VSEL Choose the supply voltage level of SIM card.

0 Supply voltage is 1.8V.

1 Supply voltage is 3V.

Signal Processing Blocks：

The main function of this block is to handle the command ordered by baseband processor about SCLK and SRST. When it receivers commands sent by SPI, it will do the corresponding signal processing, and then sent the results to analog blocks. The commands is transmitted through serial port interface (SPI) and stored in the register set. Signal processing blocks will process signals with corresponding commands. The truth table of SCLK and SRST is shown in the following tables.

Table.8-1. Truth table of SCLK

VSIM	CPOH	CPOL	SIMCLK	SCLK
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	Not allowed
1	1	0	1	Not allowed

8 Detailed Description(Continued)

1	1	1	0	1
1	1	1	1	1

Table.8-2. Truth table of SRST

VSIM	RSTSEL	RSETVAL	SIMRST	SRST
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

8.3 Analog Blocks

This module contains SIM LDO, level shifter and bandgap function. It will accept the command set by SPI and also transfer the signals to suitable voltage level to SIM cards. The SIM LDO is a regulator that could source 40mA(max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules(SIM) card.

8.4 SIM Card Interface

The SIM card interface circuitry of GT4302 meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output.

8.5 Card Activation and Deactivation

The role of GT4302 at card activation and deactivation is just a signal bypasser. It will bypass SIMCLK and SIMRST transmitted by baseband processor and turn on the channel between SIMIO and SIO.

When card activation, user just needs to follow the steps listed below.

1.Set VSEL to desired level.

2.Turn on VCCEN and DATAEN in sequence, and the other registers just keep their default settings.

3.Turn on SIM interface of baseband processor to start activation sequence.

Similarly, when card deactivation, user just follows the steps listed below.

8 Detailed Description(Continued)

1.Turn off SIM interface of baseband processor to start deactivation sequence.

2.Set DATA_L and then turn off VCCEN, and the other registers just keep their default settings.

9 Application Note

The GT4302 is a dual-channel SIM card power management and level shifter that provides 1.8V and 3.0V SIM card power for GSM and LTE cell phones with digital signal level shifting1.8V and 3.0V SIM card power supplies for GSM and LTE cellular phones with digital signal level conversion.

9.1 Typical Application

Fig.9-1 shows how the GT4302 is used. And the GT4302 requires four capacitors to operate. One input bypass capacitor is required for each of the two power supplies VIO and VBAT, and a capacitor with a capacitance of 1μF is recommended. One output bypass capacitor is required for each of the two power supplies VSIM1 and 2, which output to the SIM card, and a capacitor with a capacitance of 1μF is recommended. Capacitor type Considering the performance and space-constrained applications such as cellular phones, X5R and X7R ceramic capacitors are recommended.

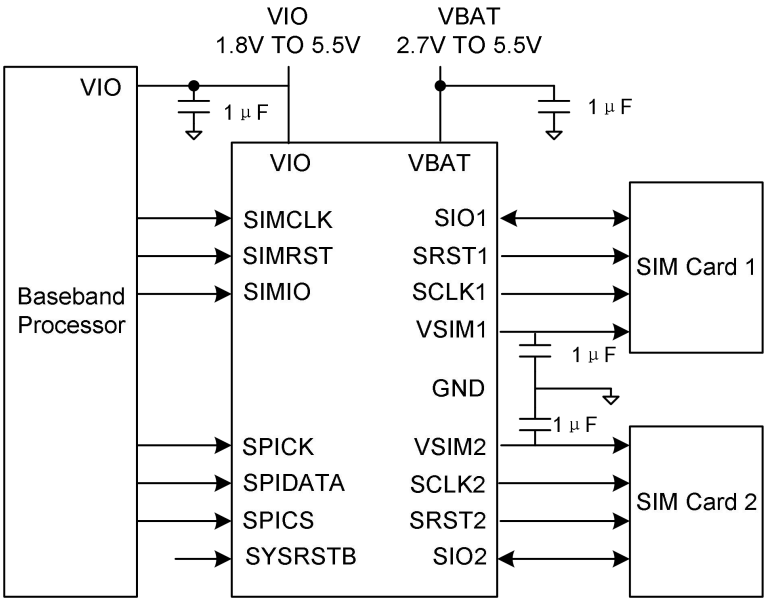


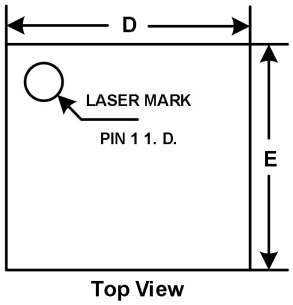
Fig.9-1. Typical application circuit

9.2 PCB layout and device layout considerations

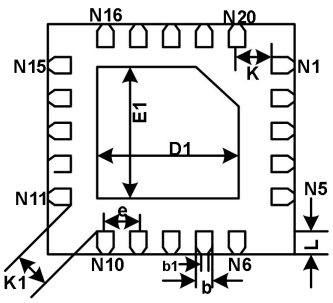
In order to fully utilize the performance of the GT4302, the PCB layout and device layout must be carefully considered. It is recommended to use a large area of PCB ground, the GT4302 adopts a 20-pin QFN 3mmX3mm package, and the exposed pads of the GND pins on the bottom of the chip should be directly connected to the ground layer of the PCB board in the form of a ground layer. The four capacitors connecting the four power supplies (VIO, VBAT, VSIM1, VSIM2) to the GND should be as close as possible to the corresponding pins of the chip, and the GND should be connected directly to the bottom layer of the PCB board, so as to minimize the ripple voltage and noise.

10 Package Outline Dimension

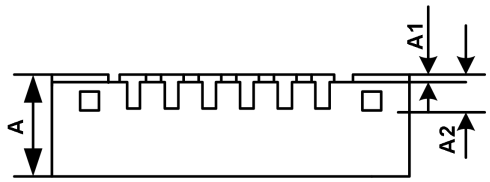
QFN3×3-20L



Top View



Bottom View



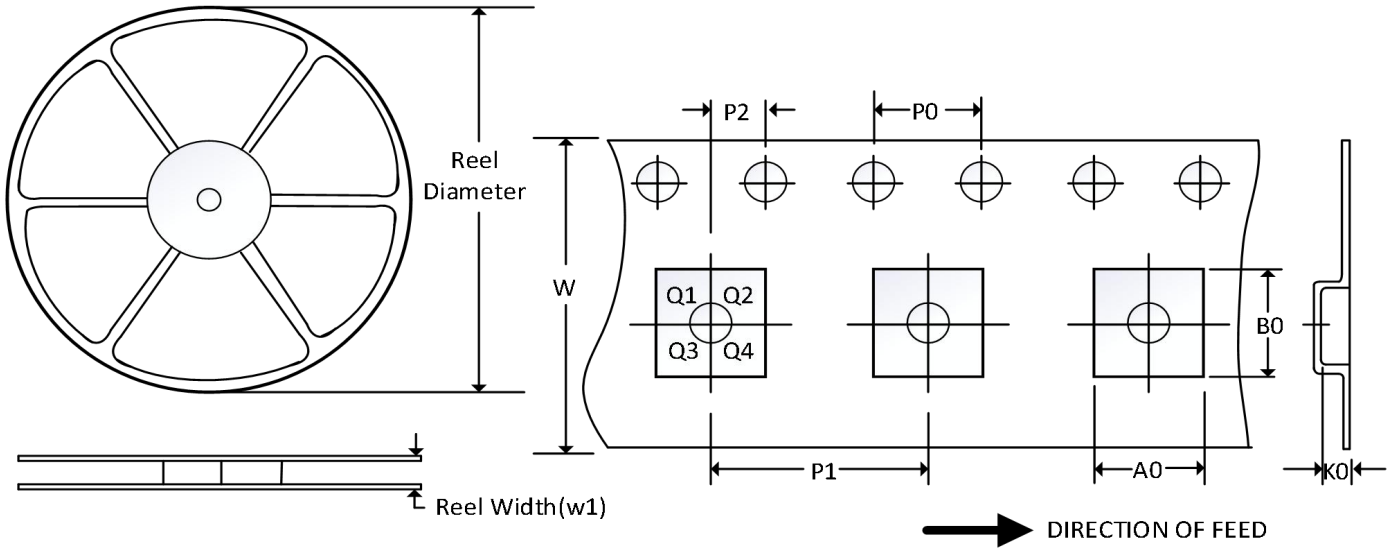
Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203REF		0.008REF	
D	2.950	3.050	0.116	0.120
E	2.950	3.050	0.116	0.120
D1	1.550	1.650	0.061	0.065
E1	1.550	1.650	0.061	0.065
K	0.300REF		0.012REF	
K1	0.400REF		0.016REF	
b	0.150	0.250	0.006	0.010
b1	0.150REF		0.006REF	
e	0.400BSC		0.016BSC	
L	0.350	0.450	0.014	0.018

11 Tape and Reel Information

Reel Dimensions

Reel Dimensions



Note: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
QFN3×3-20L	13”	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.